CLAIMS

What is claimed is:

1. A method of transferring units of information between clock domains in a memory system, the method comprising:

loading a respective set of N units of information from an output circuit in a first clock domain into a storage circuit in a second clock domain during each clock cycle of the first clock domain; and

the output circuit selecting each respective set of N units of information to include

units of information that have previously been loaded into the storage circuit and that will not be output from the storage circuit prior to the storage circuit being loaded with a subsequent set of N units of information, and

a complement number of units of information that have not previously been loaded into the storage circuit.

2. The method of claim 1 wherein the storage circuit is a shift circuit and wherein units of information are shifted out of the shift circuit in response to transitions of a clock signal in the second clock domain.

3. The method of claim 1 further comprising generating a count value that indicates how many units of information M of each set of N units loaded into the storage circuit will be output from the circuit prior to the storage circuit being loaded with a subsequent set of N units of information, wherein the complement number of units of information

includes M units of information.

4. The method of claim 3 wherein the count value is regenerated for each clock cycle of the first clock domain.

5. The method of claim 4 wherein the count value remains constant over time if the frequency of the second clock domain is an integer multiple of the frequency of the first clock domain.

6. The method of claim 4 wherein the count value varies over time if the frequency of the second clock domain is not an integer multiple of the frequency of the first clock domain.

7. The method of claim 3 wherein M is determined based on relative clock frequencies of first clock domain and the second clock domain.

8. The method of claim 1 wherein selecting each respective set of N units of information comprises selecting units of information from one or more of a plurality of information sources.

9. The method of claim 8 wherein selecting units of information from one or more of a plurality of information sources comprises selecting units of information from one or more of an information queue, a set of hold registers and a source of null data.

10. The method of claim 9 wherein the plurality of information sources further comprises a bypass source that bypasses the information queue.

11. The method of claim 1 wherein selecting each respective set of N units of information comprises issuing select signals to steering logic 83 to select a respective one of a plurality of sources to supply each unit of information in each respective set of N units of information.

12. A method of transferring units of information between clock domains in a memory system, the method comprising:

loading a first set of N units of information from an output circuit in a first clock domain into a shift circuit in a second clock domain during a first clock cycle of the first clock domain;

generating a count value, the count value indicating how many units of information M of the first set of N units of information will be shifted out of the shift circuit prior to the shift circuit being loaded with a second set of N units of information in a second clock cycle of the first clock domain; and

loading the second set of N units of information from the output circuit into the shift circuit during the second clock cycle, the second set of N units including M units of information not previously loaded into the shift circuit and N-M units of information from the first set of N units of information.